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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/702,202	10/30/2000	Peter Korger	5201-23000	9450

24319 7590 02/03/2004

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	5

DATE MAILED: 02/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/702,202	Applicant(s) KORGER, PETER	
	Examiner Shane M Thomas	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-10,12-16 and 18-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 18-20* is/are allowed.

6)☒ Claim(s) *1,2,5,6,10 and 12-14* is/are rejected.

7)☒ Claim(s) *7-9 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The Examiner respectfully withdraws his objections to Applicant's Figures 1b and 2; however, the Examiner maintains his rejection that Applicant's Figure 1a and should be designated by a legend such as --Prior Art--. The Applicant has requested that the Examiner cite prior art that contains figures identical to figures 1a and 1b. The Examiner refers to Kwon (U.S. Patent No. 5,768,546) figure 1, element 42 as being identical to Applicant's figure 1a. Column 1, lines 31-41, explicitly state that data words and respective tag bits for each byte of the data words are depicted in 42 figure 1. Further, the Examiner would like to cite figure 5 of Fukushima (U.S. Patent No. 5,748,947), which shows the configuration of data input from a FIFO (column 4, lines 1-3) as being practically identical to that of Applicant's figure 1a.

See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

The Examiner respectfully withdraws the claim objections for amended claims 10 and 18.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The Examiner's rejections for claims 1-15 and 17-19 under §112, second paragraph, have been hereto respectfully withdrawn.

Amended claims 5-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per amended claim 5, the amended claim claims dependency to canceled claim 3. Amended claims 6-9 are rejected as being dependent on rejected claim 5. For the purposes of examination, the Examiner will interpret amended claim 5 and being dependent on claim 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,5,6,10,12,13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (U.S. Patent No. 6,408,409) in view of the Applicant's admitted prior art. As per claim 1, Williams shows in figure 4 a FIFO 108 (implemented as a ring buffer) comprising 8 storage locations, an 8-bit *read register* (bits 420-428), and an 8-bit *write register* (bits 220-228). Each bit of the read and write registers corresponds one-to-one with a storage location of the FIFO buffer.

Williams does not specifically show a logic gate that is associated with each of the storage locations of the FIFO that compares the respective read and write bits of each storage location in order to determine which locations have been written to in lieu of being read from. However, as is known in the art, a FIFO storage location must be written with valid data before it is to be read (in other words, the read pointer should never advance past the write pointer, else invalid data would be read out, underflow condition). Thus, regarding decision block 526 of figure 5B, the examiner is interpreting the --time to read-- indication to read data only when valid data has been written into the corresponding storage location. In order to determine when a data block is ready to be read, it would have been obvious to one having ordinary skill in the art to have used a logic gate between the read and write bits of a respective entry in order to have

determined if the storage location should be read (i.e. when the storage location had been written to with data, but the data had not been read out yet). For example, it would have been obvious for the Time-to-Read block 526 to have used an XOR gate in order to have determined disparity between the read and write bits of an entry and then used the output of that logic gate to either follow the --No-- branch (data not yet ready to be read) or the --Yes-- branch (data ready to be read, block 528).

Williams does not teach associated tag bits with each data entry. The Applicants admitted prior art teaches in page 2, lines 5-12, of the disclosure that tag bits associated with FIFO data can be used to facilitate data transfer by reducing the amount of processing required at the receiving of the FIFO buffer. Thus it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the FIFO ring buffer of Williams with the teaching of tag bits of the Applicant's in order to have attached a *T* number of tag bits with each data entry being written into the FIFO, which would have increased the throughput of the computer system 100 using the FIFO ring buffer of Williams by decreasing the amount of processing time spent ascertaining the nature of the data in the transfer (data written into the FIFO). The Examiner is regarding the --status-- of the storage locations of the FIFO ring buffer to be which kind of transfer (from a particular source of the plurality of sources mentioned by Williams in column 3, lines 50-55). The Applicant's admitted prior art states on page 2, line 8 that tag bits can be used to indicate which source sent data to the FIFO; therefore, the Examiner is interpreting that different combinations of active tag bits will indicate different sources of data (such as data from an I/O device would have a different tag than data from a memory device - column 3, lines 53-54). Thus it could have been seen that that --status-- or which source data

being written into the FIFO originated from would have depended on whether *respective tag bits were active.*

As per claim 2, Williams shows in figure 4 that data is being transmitted into the FIFO buffer 108 with transmit clock 106 (*first clock*) and being read from buffer 108 with receive clock 110 (*second clock*).

As per claims 5 and 13, the Examiner will refer to storage locations that have been written to but not read as --valid-- storage locations since they are the only locations in the FIFO that contain data yet to be read.

As per claims 6 and 14, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used combinatorial logic in order to have been able to trasmit the logic level (--status--) of the tag bits of the data entry being read out of a FIFO entry in order to have facilitated the data transfer as was associated with the benefit of utilizing tag bits according to the Applicant's admitted prior art. In other words, combinatorial logic would have enabled the computer system to distinguish one set of tag bits from another, which would represent distinguishing one source of data from another source of data that had written data into the FIFO 108. Further it would have been seen to one of ordinary skill in the art that the the tag bits could have been read out from any of the 8 storage locations in the FIFO, depending which location was currently being read. This location would have been valid since ascertaining the logic level of the tag bits for an invalid entry would have been unnecessary; thus, the computer system 100 of essential would have *ignored* the tags bits of invalid FIFO storage locations.

As per claim 10, the rejection for lines 1-3 follows the rejection for claim 1, lines 1-2. The rejection for lines 4-5 follows the rejection for claim 2. The rejection for lines 6-8 follows

the rejection for claim 1, lines 3-4. Finally, the rejection for lines 9-10 follows the rejection for claim 1, lines 8-9.

As per claim 12, the rejection follows the rejection for claim 1, lines 5-8 wherein the Examiner is considering the --combinatorial logic-- of claim 12 as being equivalent to the --logic gate-- of claim 1.

Response to Amendment

As per amended claims 1 and 10, the Examiner has applied the prior art reference of Williams et al. (U.S. Patent No. 6,408,409) to reject claims 1,2,5,6,10, and 12-14, necessitated by the Applicant's amendment to claim 1, lines 3-4 and claim 10, lines 6-8.

Response to Arguments

Applicant's arguments, see pages 7-8, filed 18 November 2003, with respect to figures 1a and 1b not being designated as prior art have been fully considered and are persuasive for figure 1b only. The objection of figure 1b has been withdrawn. The Examiner has supplied evidence - reference to Kwon (U.S. Patent No. 5,768,549) and Fukushima (U.S. Patent 5,748,974) - in order to support the Examiner's argument for the request to label figure 1a as --Prior Art--.

Applicant's arguments, see pages 8-9, filed 18 November 2003, with respect to the term --status-- have been fully considered and are persuasive. The rejection of §112, second paragraph, has been withdrawn.

Allowable Subject Matter

Claims 7-9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Williams nor the Applicant's admitted prior art teach using combinatorial logic in accordance with the manner of claim 7.

Claims 15-20 are allowable. The following is a statement of reasons for the indication of allowable subject matter: the prior art reference of Williams teaches lines 1-18 of claim 16; however, Williams nor the Applicant's admitted prior art teach generating logic signals such that the i^{th} logic signal is active (logic 1) if *any* of the i^{th} tag bits are active. The reasons for the allowability of claim 15 follow the reasoning of claim 16, lines 19-20, stated directly above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (703) 605-0725. The examiner can normally be reached on M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 764-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Shane M. Thomas

MATTHEW KIM
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